Measurement of interface-state parameters near the band edge at the Si/SiO2 interface by the conductance method

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Measurement of interface-state parameters near the band edge at the Si/SiO_2 interface by the conductance method

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The interface-state parameters near the band edge at the Si/SiO_2 interface were measured using the MOS conductance method with the reflection technique, extending the frequency up to 100 MHz. The double peaks were observed in the conductance-vs-frequency curves. The decrease of the capture cross section toward the band edge was found due to the overlap of the double peaks. The new peak at higher frequencies suggests the existence of new interface states, which has been overlooked so far.

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The properties of interface states near the band edge at the Si/SiO_2 interface have not been fully understood in contrast to those near the midgap. Study of the interface states was first carried out by Gray and Brown[1] using the low-temperature technique; but the Gray-Brown technique could not provide information about the capture cross section. Fahner *et al.*[2] measured the physical parameters of the interface states near the band edge using the MOS conductance method, extending the frequency up to 50 MHz, while Deuling *et al.*[3] measured the parameters in the temperature range between the liquid-nitrogen and room temperatures. They[2,3] observed that the capture cross section was independent of energy near the midgap, while it decreases exponentially with energy near the conduction band.

In order to clarify the origin of the decrease of the cross section, we have carried out the measurements of the interface-state parameters near the band edge at the Si/SiO_2 interface using the MOS conductance method with the reflection technique, extending the frequency up to 100 MHz.

The samples used were made by thermal oxidation of n-type layers (26.5 Ω cm, 9.2 μm) epitaxially grown on highly doped (111) substrates. Oxidations were carried out at 1050 °C for 3 h in a dry O_2 (100 ppm H_2O) atmosphere. The thickness of oxide was about 900 Å. Low-temperature annealing was done at 400 °C for 30 min in a dry N_2 (100 ppm H_2O) atmosphere, after Al electrodes 1 mm in diameter were evaporated. The reasons for the use of the epitaxial layer on the highly doped substrate are as follows. First, we need a good back Ohmic contact for the high-frequency measurements. Second, the total bulk resistance should be as small as possible to obtain accurate values of the conductance component due to interface states.

The impedance of MOS capacitors was measured using the Hewlett Packard 8405A vector voltmeter in the frequency range from 1 to 100 MHz. A block diagram of the setup for making the reflection measurements is shown in Fig. 1(a). The use of a directional bridge gives the accurate correction values of the circuit constants determined by a short condition at the sample port in the low-frequency region. When the frequency is higher than about 1 MHz, the equivalent circuit of the line must be described by the distributed constant circuit because the wavelength of the signal cannot be negligible compared with the size of the circuit elements. The equivalent circuit of the line between the B-channel probe tee and the sample port is given in Fig. 1(b). The correction factors including the circuit constants are determined by the relations

$$\exp(2\gamma_n l_n) = -1/\rho_n^{(s)},$$

$$\rho_n^{(s)} = (V_{nr}/V_{ni})_{\text{short}},$$

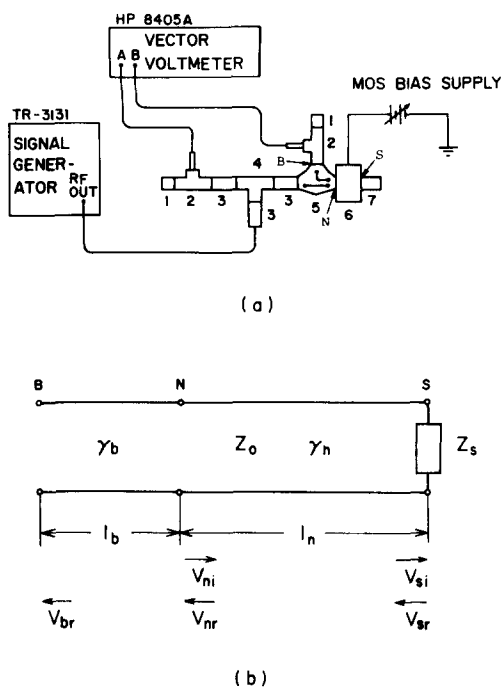

FIG. 1. (a) Block diagram of apparatus for the reflection measurements. 1: 50-Ω load, 2; probe tee, 3: coaxial attenuator, 4: power splitter, 5: directional bridge, 6: bias network, 7: sample. (b) Equivalent circuit of the line between the B-channel probe tee and the sample port for the reflection measurements. Z_0: characteristic impedance of the line, Z_s: load (sample) impedance, γ_b and l_b: propagation constant and line length between the B port and the N port, respectively, γ_n and l_n: propagation constant and line length between the N-port and the sample port, respectively, V_{br}: reflected voltage at the B port, V_{ni} and V_{nr}: incident and reflected voltages at the N port, respectively, V_{si} and V_{sr}: incident and reflected voltages at the sample port, respectively.

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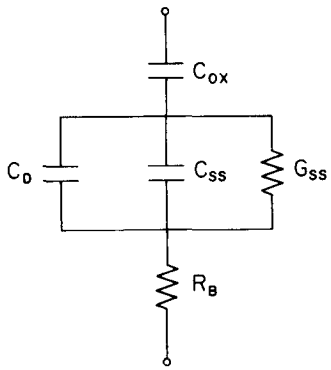

FIG. 2. Equivalence circuit of the MOS capacitor. C_{ox}: oxide capacitance, C_D: depletion layer capacitance, C_{ss}: capacitance of interface states, G_{ss}: conductance of interface states, R_B: bulk resistance.

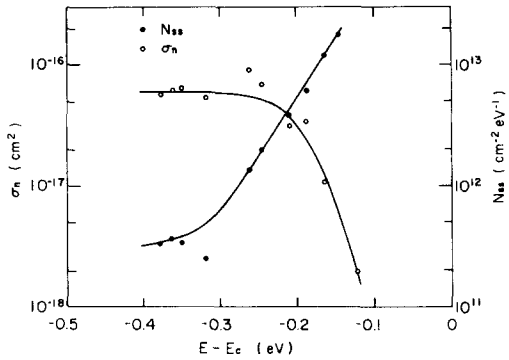

FIG. 4. Apparent interface-state density N_{ss} and apparent electron capture cross section σ_n of interface states as a function of the energy. The energy is measured relative to the conduction-band edge.

where γ_n is the propagation constant, l_n is the line length between the N port and the sample port, V_{ni} and V_{nr} are the incident and reflected voltages at the N port, respectively, and $\rho_n^{(s)}$ is measured by placing a short circuit at the sample port. The amplitude of applied rf voltage at the sample port was approximately 8 mV.

In the frequency range from 5 Hz to 100 kHz, the capacitance and the conductance were measured using the phase-sensitive detection with the Princeton Applied Research 124 lock-in amplifier, while in the frequency range from 5 to 500 kHz the measurements were carried out using the Boonton Electronics 75C capacitance bridge.

The parameters of the interface states were evaluated using the MOS conductance method.[4] The equivalent circuit of the MOS capacitor is given in Fig. 2. It should be noted that the contribution of the bulk resistance to the impedance of the entire MOS capacitor increases as the frequency increases. The information on the interface states can be obtained from the characteristic curves of G_{ss}/ω versus $\log f$, where G_{ss} is the conductance and ω $(=2\pi f)$ is the angular frequency. Figure 3 shows the measured G_{ss}/ω-vs-$\log f$ curves with the field-plate bias as a parameter. The double peaks have been observed. The peak in the low-frequency range is the peak observed before.[2,3] If we disregard the existence of the high-frequency peak and take only the low-frequency peak into consideration, we obtain an apparent interface-state density and an apparent electron capture cross section near the conduction-band edge as shown in Fig. 4, which is very similar to the figures obtained by Fahner *et al.*[2] and by Deuling *et al.*[3] Therefore, we conclude that the decrease of the electron capture cross section toward the conduction-band edge reported so far is caused by the existence of the new peak at the high-frequency range which has been overlooked so far.

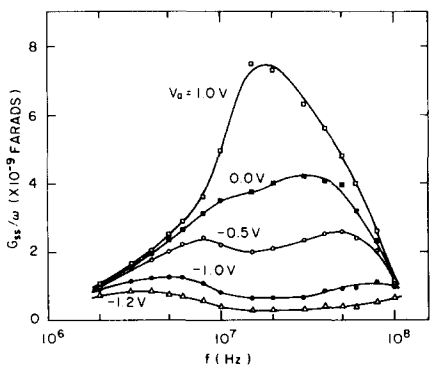

FIG. 3. G_{ss}/ω-versus log$f$ with field-plate bias as parameters. Flatband voltage is -1.6 V.

Let us consider the possible origin of the new peak in Fig. 3. One possibility is that the new peak indicates the existence of new interface states. The characteristic features of the new peak are as follows. The peak values increase linearly with bias voltage toward accumulation and the positions of the peak shift toward lower frequencies. This behavior cannot be explained by the models so far proposed.[4-6] Therefore, it is likely that the new peak suggests the new interface states which cannot be described by the conventional models.

Another possibility is that the new peak appears to be due to the inaccuracy of the values of the bulk resistance. In the investigations of interface states near the band edges so far reported, there is no discussion of the effect of the bulk resistance. However, the contribution of the bulk resistance to the impedance of the entire MOS capacitor increases as the frequency increases. Thus, we need a very accurate value of the bulk resistance in order to obtain accurate values of G_{ss}/ω we have used the value of the bulk resistance estimated by the bulk resistivity $\rho = 26.5\ \Omega$cm. This value of the resistivity was calculated using the doping density of the epitaxial layer determined by the C-V method. This value is roughly equal to the values (23.7–32.4 Ωcm) obtained by the monitor substrates. The monitor substrates consist of the n-type layer epitaxially grown on the p-type substrates under the same condition as that under which the n-type layer is epitaxially grown on highly doped n-type substrates. It is easy to measure the resistivity of the n-type layer of the monitor substrates. In the high-frequency range, the curves of G_{ss}/ω reflect changes in the the values of the bulk resistance. However, the new peaks always

exist for $\rho = 23.7-32.4\ \Omega$cm. Therefore, it is not likely that the new peak appears to be due to the inaccuracy of the value of the bulk resistance.

In conclusion, we have obtained the results which show that the decrease of the capture cross section of the interface states at the Si/SiO_2 interface toward the band edge is due to the overlap of double peaks in the interface-state conductance curves. We believe that the new peak at higher frequencies suggests the existence of new interface states overlooked so far.

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Surface potential of anodized *p*-GaAs MOS capacitors

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Metal-oxide-semiconductor (MOS) capacitors were constructed on *p*-type GaAs anodized in a tartaric acid-water-glycol solution at room temperature, and capacitance-voltage measurements were made on them from the quasistatic regime to 150 MHz. The data thus obtained indicate that the zero-bias surface potential is 0.59 V, that the total surface potential excursion is limited to ~0.45 V, and that neither flatband nor inversion were achievable. The minimum in surface-state density was $\sim 4\times 10^{12}$ cm^{-2}eV^{-1}.

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Previously reported capacitance-voltage (C-V) measurements[1] on *p*-type GaAs have implied that surface accumulation and inversion are reached and that a surface-state density of $\sim 10^{11}$ cm^{-2} eV^{-1} exists near midgap. This conclusion was based on a 1-MHz measurement of the C-V characteristics of MOS capacitors and an analysis using the Terman method,[2] with the assumption that no surface states were responding to the measurement frequency. C-V measurements made at 150 MHz on *n*-GaAs capacitors have indicated that large numbers of surface states can, in fact, respond to frequencies above 1 MHz on *n*-type material,[3] and more-recent results on *p*-type GaAs have indeed indicated that a true high-frequency C-V curve is not obtained at 1 MHz.[4,5]

This letter reports the results of C-V measurements made on anodically formed *p*-GaAs MOS capacitors from the quasistatic regime to 150 MHz. The devices were made using Cd-doped $p = 2.3\times 10^{17}$-cm^{-3} ⟨100⟩-oriented substrates. These were cleaned in hot 45% KOH, rinsed in deionized water, etched in 1% Br-methanol, and rinsed in deionized water immediately prior to anodization. Anodization was performed at 100 μA/cm^2 in a 3 wt% aqueous solution of tartaric acid buffered to a pH of 6.0 and mixed in a ratio of 1:3 with propylene glycol. The samples were then annealed at 400 °C for 12 min in an atmosphere of 8.5% H_2 in He and thinned to ~0.1 mm to reduce the series resistance of the substrate. Aluminum gates were evaporated through a metal mask, and a soldered 80% In—20% Cd contact was applied to the back of the sample before again alloying for 1 min at 400 °C.

The measurements were performed in the same manner as previously described[3] and the results are shown in Fig. 1. The devices all exhibited a counterclockwise hysteresis; however, only the negative-going sweep is shown for clarity. A large dispersion in the oxide dielectric constant appears to occur between 10 Hz and the quasistatic data. The analysis of the quasistatic data was accomplished using a different value of oxide capacitance than that used for the high-frequency data. Integration of the area below a horizontal line drawn through C_{ox} and the experimental curve for the quasistatic data as described by Berglund[6] yields a total change in surface potential of 0.45 V. The carrier concentration for this device was determined from a deep depletion curve taken with a sweep rate of 400 V/sec. The doping density was calculated from the plot of the measured deep depletion capacitance C_m versus gate voltage V_g in Fig. 2 using the method of van Gelder and Nicollian.[7] Using the equation

$$N_A = 2\left(q\epsilon_s \frac{d(A/C_m)^2}{dV_g}\right)^{-1}, \tag{1}$$

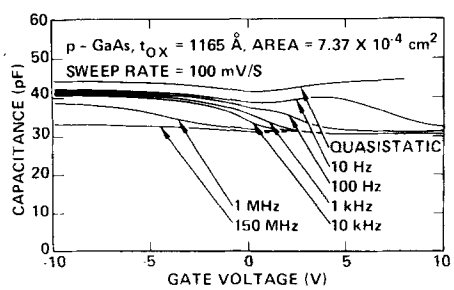

FIG. 1. Capacitance-voltage characteristics of anodized *p*-GaAs.

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